

IN THE CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1        1. (Currently Amended) A configurable integrated circuit comprises:

2                at least one general purpose input/output (GPIO) interface module that includes a plurality of  
3        GPIO cells, wherein a GPIO cell of the plurality of GPIO cells is operably coupled to a corresponding pin  
4        of the configurable integrated circuit, wherein, when the configurable integrated circuit is in a first  
5        functional mode, the GPIO cell is operably coupled to the corresponding pin such that the corresponding pin  
6        functions as a digital input pin and when the configurable integrated circuit is in a second functional  
7        mode, the GPIO cell is operably coupled to the corresponding pin such that the corresponding pin  
8        functions as a digital output pin;

9                a first functional module having a connection operably coupled to the GPIO cell when the  
10      configurable integrated circuit is in the first functional mode; ~~and~~

11                ~~a second~~ ~~second~~ functional module having a connection operably coupled to the GPIO cell when  
12      the configurable integrated circuit is in the second ~~functional state~~ ~~functional mode~~; ~~and~~

13                ~~programmable logic fabric operably coupled between the at least one GPIO interface module and~~  
14        ~~the first or second functional module.~~

2. (Cancelled)

1        3. (Currently Amended) The ~~configuration~~ ~~configurable~~ integrated circuit of ~~claim 2~~ ~~claim 1~~  
2      further comprises:

3                remaining GPIO cells of the plurality of GPIO cells are operably coupled to the programmable  
4        logic fabric, wherein the programmable logic fabric is programmed to provide at least one of:

5                coupling between at least some of the remaining GPIO cells and corresponding pins of a set of  
6        pins of the configurable integrated circuit;

7                processing of inbound digital signals when the configurable integrated circuit is in the first  
8        functional mode; and

9                processing of outbound digital signals when the configurable integrated circuit is in the second  
10      functional mode.

1       4. (Currently Amended) The configurable integrated circuit of claim 1, wherein the first  
2 ~~function~~ functional module and second ~~function~~ functional module comprises at least one of:  
3       a liquid crystal display (LCD) interface module;  
4       a light emitting diode (LED) interface module;  
5       a random access memory (RAM) interface module;  
6       a compact disk (CD) control interface module;  
7       flash memory module;  
8       hard drive;  
9       random access memory (RAM) module;  
10      a two-wire interface module; and  
11      a system packet interface module.

1       5. (Original) The configurable integrated circuit of claim 1, wherein each of the plurality of  
2 GPIO cells comprises:  
3       a data input buffer having an input and an output, wherein the input of the data input buffer is  
4 operably coupled to the corresponding pin;  
5       a data output buffer having an input and an output, wherein the output of the data output buffer is  
6 operably coupled to the corresponding pin;  
7       a data input connection operably coupled to, when enabled, provide an inbound data signal from  
8 the output of the data input buffer to the first functional module;  
9       a data input register operably coupled to, when enabled, store the inbound data signal for  
10 subsequent access by a processing core;  
11      a data output connection operably coupled to, when enabled, provide an outbound data signal  
12 from the second functional module to the input of the data output buffer;  
13      a data output register operably coupled to, when enabled, provide an alternate outbound data  
14 signal to the input of the data output buffer; and  
15      an input/output selection module operably coupled to enable at least one of the data input buffer,  
16 the data output buffer, the data input connection, the data input register, the data output connection, and  
17 the data output register.

1        6. (Original) The configurable integrated circuit of claim 5, wherein the input/output  
2 selection module comprises:

3            a first control register operably coupled to store a multiplexer selection signal;

4            a second control register operably coupled to store an overwriting enable/disable signal;

5            a first multiplexer operably coupled to provide the outbound data signal to the input of the data  
6 output buffer when the multiplexer selection signal is in a first state and to provide the alternate output  
7 data signal to the input of the data output buffer when the multiplexer selection signal is in a second state;  
8 and

9            a second multiplexer operably coupled to provide an output enable signal to the data output buffer  
10 when the multiplexer selection signal is in a third state and to provide the overwriting enable/disable  
11 signal to the data output buffer when the multiplexer selection signal is in a fourth state.

1        7. (Currently Amended) The configurable integrated circuit of claim 6 further comprises:

2            the multiplexer selection signal being in the first state and the third state simultaneously, the first  
3 state and the fourth state simultaneously, the second state and the third state simultaneously, or the second  
4 state and the fourth state simultaneously.

1        8. (Original) The configurable integrated circuit of claim 1, wherein the at least one general  
2 purpose input/output (GPIO) interface module further comprises:

3            a first GPIO interface module operably coupled to the first and second functional modules; and

4            a second GPIO interface module operably coupled to a third functional module and a fourth

5 functional module, wherein, when the configurable integrated circuit is in a third functional mode, a  
6 GPIO cell of the second GPIO interface module is operably coupled to a second corresponding pin such  
7 that the second corresponding pin functions as a digital input pin and when the configurable integrated  
8 circuit is in a second functional mode, the GPIO cell of the second GPIO interface module is operably  
9 coupled to the second corresponding pin such that the second corresponding pin functions as a digital  
10 output pin.

1           9. (Currently Amended) A configurable general purpose input/output (GPIO) comprises:  
2            a first GPIO cell operably coupled to a first pin of an integrated circuit to receive first input  
3            signals from the first pin and provide the first input signals to a first circuit when a mode selection signal  
4            is in a first state and to provide the first input signals to a first register when the mode selection signal is  
5            in a second state, wherein the first GPIO GPIO cell is further operably coupled to provide first output  
6            signals from a second circuit to the first pin when the mode selection signal is in a third state and to  
7            provide first alternate output signals from a second register to the first pin when the mode selection signal  
8            is in a fourth state; and

9            a second GPIO cell operably coupled to a second pin of the integrated circuit to receive second  
10          input signals from the second pin and provide the second input signals to a third circuit when a second  
11          mode selection signal is in a first state and to provide the second input signals to a third register when the  
12          second mode selection signal is in a second state, wherein the second GPIO GPIO cell is further operably  
13          coupled to provide second output signals from a fourth circuit to the second pin when the second mode  
14          selection signal is in a third state and to provide second alternate output signals from a fourth register to  
15          the second pin when the second mode selection signal is in a fourth state.

1           10. (Original) The configurable GPIO of claim 9, wherein the first GPIO cell comprises:  
2            a data input buffer having an input and an output, wherein the input of the data input buffer is  
3          operably coupled to the first pin;  
4            a data output buffer having an input and an output, wherein the output of the data output buffer is  
5          operably coupled to the first pin;  
6            a data input connection operably coupled to, when enabled, provide the first input signals from  
7          the output of the data input buffer to the first circuit;  
8            the first register operably coupled to, when enabled, store the first input signals for subsequent  
9          access by a processing core;  
10          a data output connection operably coupled to, when enabled, provide the first output signals from  
11          the second circuit to the input of the data output buffer;  
12          the second register operably coupled to, when enabled, provide the first alternate output signals to  
13          the input of the data output buffer; and  
14          an input/output selection module operably coupled to enable at least one of the data input buffer,  
15          the data output buffer, the data input connection, the first register, the data output connection, and the  
16          second register.

1           11. (Original) The configurable GPIO of claim 10, wherein the input/output selection module  
2 comprises:

3           a first control register operably coupled to store a multiplexer selection signal;

4           a second control register operably coupled to store an overwriting enable/disable signal;

5           a first multiplexer operably coupled to provide the first output signals to the input of the data  
6 output buffer when the multiplexer selection signal is in a first state and to provide the first alternate  
7 output signals to the input of the data output buffer when the multiplexer selection signal is in a second  
8 state; and

9           a second multiplexer operably coupled to provide an output enable signal to the data output buffer  
10 when the multiplexer selection signal is in a third state and to provide the overwriting enable/disable  
11 signal to the data output buffer when the multiplexer selection signal is in a fourth state.

1           12. (Original) The configurable GPIO of claim 9, wherein the second GPIO cell comprises:

2           a data input buffer having an input and an output, wherein the input of the data input buffer is  
3 operably coupled to the second pin;

4           a data output buffer having an input and an output, wherein the output of the data output buffer is  
5 operably coupled to the second pin;

6           a data input connection operably coupled to, when enabled, provide the second input signals from  
7 the output of the data input buffer to the third circuit;

8           the third register operably coupled to, when enabled, store the second input signals for subsequent  
9 access by a processing core;

10          a data output connection operably coupled to, when enabled, provide the second output signals  
11 from the fourth circuit to the input of the data output buffer;

12          the fourth register operably coupled to, when enabled, provide the second alternate output signals  
13 to the input of the data output buffer; and

14          an input/output selection module operably coupled to enable at least one of the data input buffer,  
15 the data output buffer, the data input connection, the first register, the data output connection, and the  
16 second register.

1        13. (Original) The configurable GPIO of claim 12, wherein the input/output selection module  
2 comprises:

3            a first control register operably coupled to store a multiplexer selection signal;

4            a second control register operably coupled to store an overwriting enable/disable signal;

5            a first multiplexer operably coupled to provide the second output signals to the input of the data  
6 output buffer when the multiplexer selection signal is in a first state and to provide the second alternate  
7 output signals to the input of the data output buffer when the multiplexer selection signal is in a second  
8 state; and

9            a second multiplexer operably coupled to provide an output enable signal to the data output buffer  
10 when the multiplexer selection signal is in a third state and to provide the overwriting enable/disable  
11 signal to the data output buffer when the multiplexer selection signal is in a fourth state.

1        14. (Original) The configurable GPIO of claim 9 further comprises at least one of:  
2            the first circuit and the second circuit being part of a functional module; and  
3            the first and second circuits being part of different functional modules.

1        15. (Original) The configurable GPIO of claim 9 further comprises at least one of:  
2            the third and fourth circuits being part of a functional module; and  
3            the third and fourth circuits being part of different functional modules.

1        16. (Currently Amended) A multiple function system on a chip integrated circuit comprises:  
2        a processing module;  
3        on-chip memory operably coupled to the processing module;  
4        memory interface for accessing off-chip memory, wherein at least of the on-chip memory and the  
5        off-chip memory store operational instructions that cause the processing module to perform at least one of  
6        a data file storage function, audio storage function, and audio playback function;  
7        a plurality of functional modules operably coupled to the processing module; and  
8        at least one general purpose input/output (GPIO) interface module operably coupled to the  
9        plurality of functional modules and the processing module, wherein the at least one GPIO includes a  
10        plurality of GPIO cells, wherein a GPIO cell of the plurality of GPIO cells is operably coupled to a  
11        corresponding pin of the multiple function system of a chip integrated circuit, wherein, when the multiple  
12        function system of a chip integrated circuit is in a first functional mode, the GPIO cell is operably coupled  
13        to the corresponding pin such that the corresponding pin functions as a digital input pin and when the  
14        multiple function system of a chip integrated circuit is in a second functional mode, the GPIO cell is  
15        operably coupled to the corresponding pin such that the corresponding pin functions as a digital output  
16        pin, wherein each of the plurality of GPIO cells comprises:  
17                a data input buffer having an input and an output, wherein the input of the data input  
18                buffer is operably coupled to the corresponding pin;  
19                a data output buffer having an input and an output, wherein the output of the data output  
20                buffer is operably coupled to the corresponding pin;  
21                a data input connection operably coupled to, when enabled, provide an inbound data  
22                signal from the output of the data input buffer to the first functional module;  
23                a data input register operably coupled to, when enabled, store the inbound data signal for  
24                subsequent access by a processing core;  
25                a data output connection operably coupled to, when enabled, provide an outbound data  
26                signal from the second functional module to the input of the data output buffer;  
27                a data output register operably coupled to, when enabled, provide an alternate outbound  
28                data signal to the input of the data output buffer; and  
29                an input/output selection module operably coupled to enable at least one of the data input  
30                buffer, the data output buffer, the data input connection, the data input register, the data output  
31                connection, and the data output register.

1           17. (Currently Amended) The multiple function system on a chip integrated circuit of claim  
2   16 further comprises:

3           programmable logic fabric operably coupled between the at least one GPIO interface module and  
4   at least one of the plurality of ~~function modules~~ functional modules.

1           18. (Original) The multiple function system on a chip integrated circuit of claim 17 further  
2   comprises:

3           remaining GPIO cells of the plurality of GPIO cells are operably coupled to the programmable  
4   logic fabric, wherein the programmable logic fabric is programmed to provide at least one of:

5           coupling between at least some of the remaining GPIO cells and corresponding pins of a set of  
6   pins of the configurable integrated circuit;

7           processing of inbound digital signals when the multiple function system of a chip integrated  
8   circuit is in the first functional mode; and

9           processing of outbound digital signals when the multiple function system of a chip integrated  
10   circuit is in the second functional mode.

1           19. (Currently Amended) The multiple function system on a chip integrated circuit of claim  
2   16, wherein the plurality of ~~function~~ functional modules comprises two or more of:

3           a liquid crystal display (LCD) interface module;

4           a light emitting diode (LED) interface module;

5           a random access memory (RAM) interface module;

6           a compact disk (CD) control interface module;

7           flash memory interface module;

8           hard drive;

9           a two-wire interface module; and

10          a system packet interface module.

20. (Cancelled)

1           21. (Currently Amended) The multiple function system on a chip integrated circuit of ~~claim~~  
2 ~~20~~ claim 16, wherein the input/output selection module comprises:

3           a first control register operably coupled to store a multiplexer selection signal;  
4           a second control register operably coupled to store an overwriting enable/disable signal;  
5           a first multiplexer operably coupled to provide the outbound data signal to the input of the data  
6           output buffer when the multiplexer selection signal is in a first state and to provide the alternate output  
7           data signal to the input of the data output buffer when the multiplexer selection signal is in a second state;  
8           and

9           a second multiplexer operably coupled to provide an output enable signal to the data output buffer  
10          when the multiplexer selection signal is in a third state and to provide the overwriting enable/disable  
11          signal to the data output buffer when the multiplexer selection signal is in a fourth state.

1           22. (Currently Amended) The multiple function system on a chip integrated circuit of claim  
2          21 further comprises:

3           the multiplexer selection signal being in the first state and the third state simultaneously, the first  
4           state and the fourth state simultaneously, the second state and the third state simultaneously, or the second  
5           state and the fourth state simultaneously.

1           23. (Original) The multiple function system on a chip integrated circuit of claim 16, wherein  
2          the at least one general purpose input/output (GPIO) interface module further comprises:

3           a first GPIO interface module operably coupled to first and second functional modules of the  
4           plurality of functional modules; and

5           a second GPIO interface module operably coupled to a third and fourth functional modules of the  
6           plurality of functional modules, wherein, when the configurable integrated circuit is in a third functional  
7           mode, a GPIO cell of the second GPIO interface module is operably coupled to a second corresponding  
8           pin such that the second corresponding pin functions as a digital input pin and when the configurable  
9           integrated circuit is in a second functional mode, the GPIO cell of the second GPIO interface module is  
10          operably coupled to the second corresponding pin such that the second corresponding pin functions as a  
11          digital output pin.